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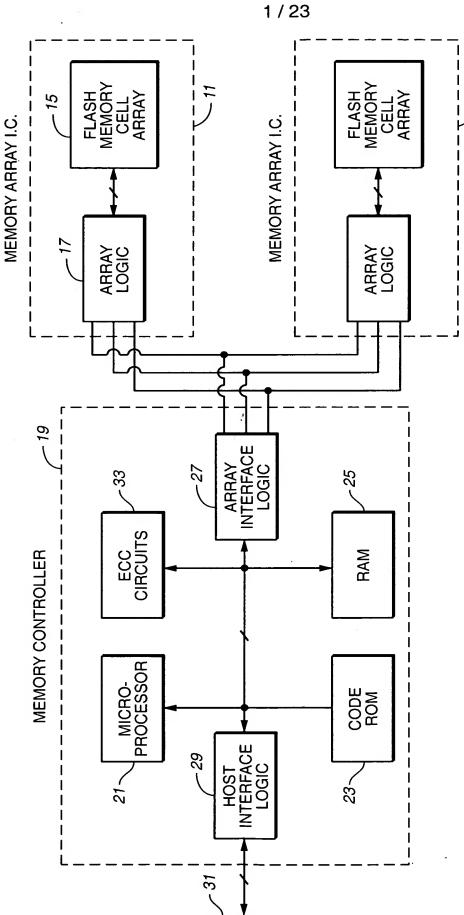
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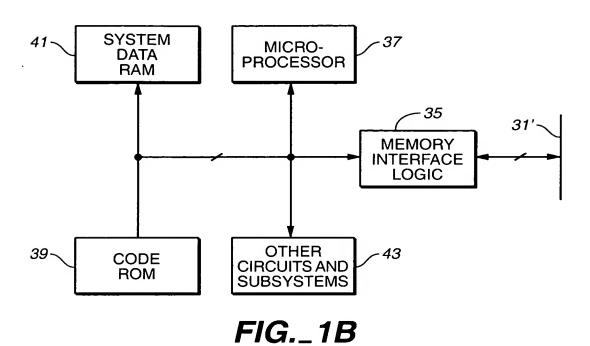
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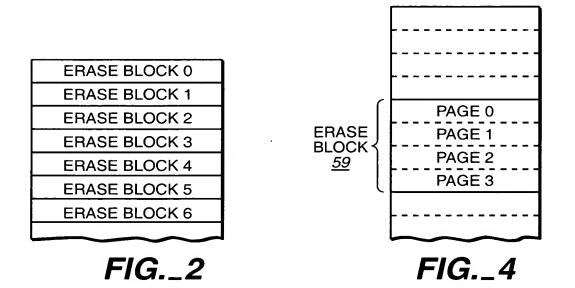


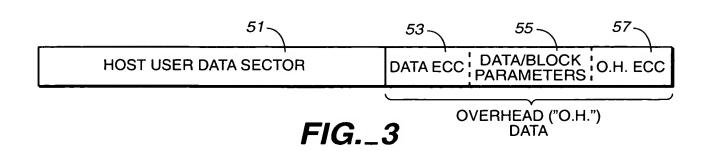
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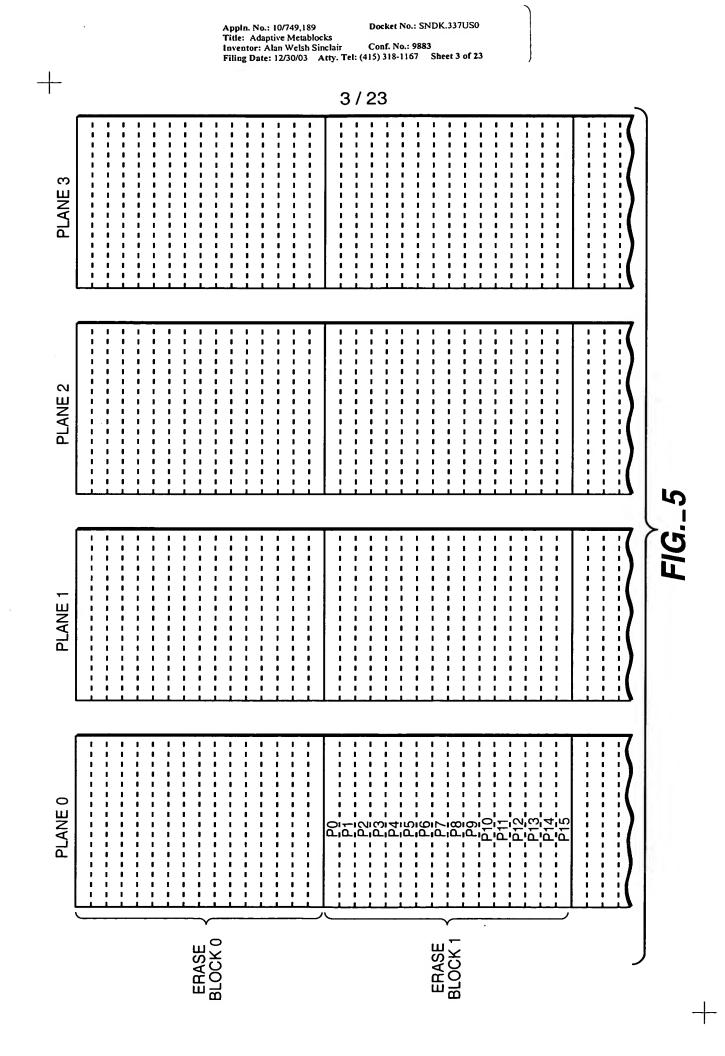
Inventor: Alan Welsh Sinclair Conf. No.: 9883
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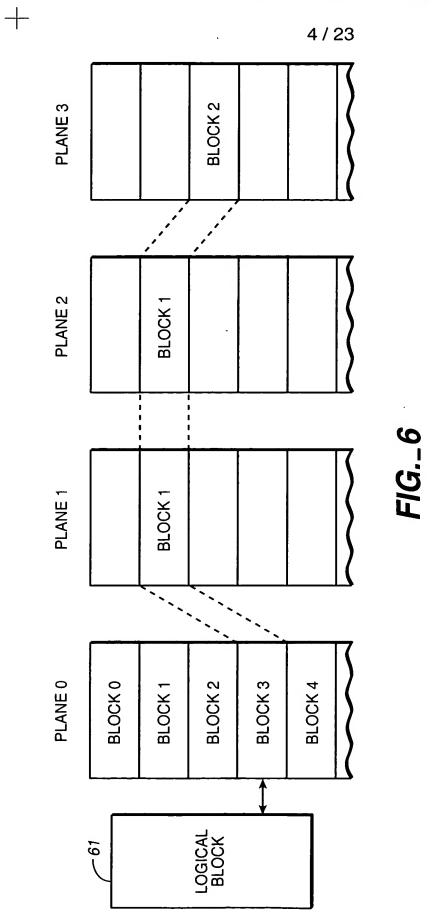


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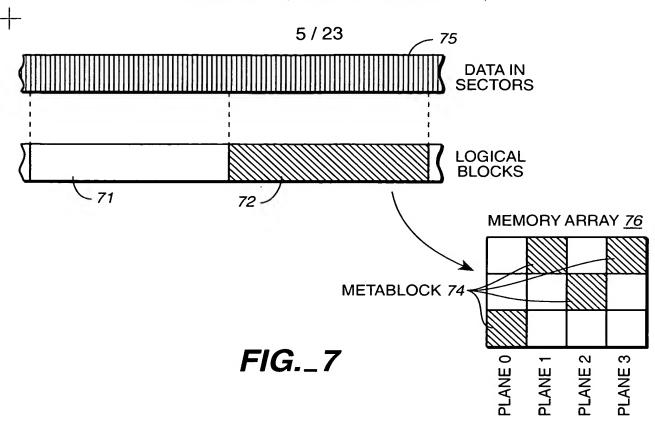
 Inventor: Alan Welsh Sinclair
 Conf. No.: 9883

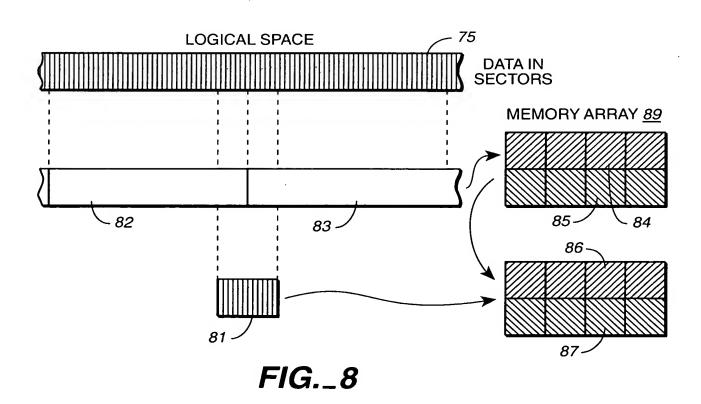
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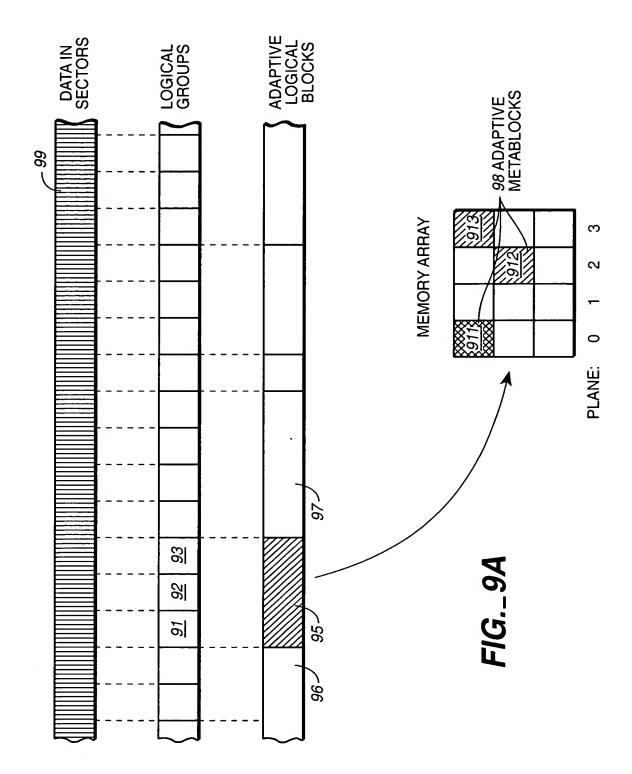
Appln. No.: 10/749,189 Docket No.: SNDK.337US0
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Conf. No.: 9883

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Title: Adaptive Metablocks
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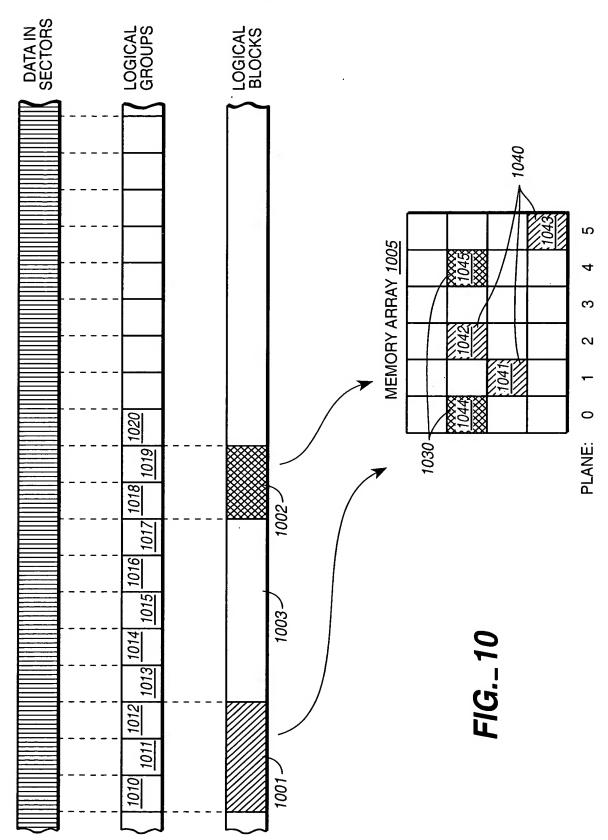


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DATA IN SECTORS	LOGICAL						
3n+2 3n+1 3n 3n-1							
3n-1	<u>83</u>						
2n+2 2n+1 2n 2n-1			AL BLOCK <u>95</u>				
n+2 n+1 n	<u>85</u>		ADAPTIVE LOGICAL BLOCK <u>95</u>				
n-1 4 3 2 SECTOR 1	<u>91</u>		AD				
SECTOR 1		 					

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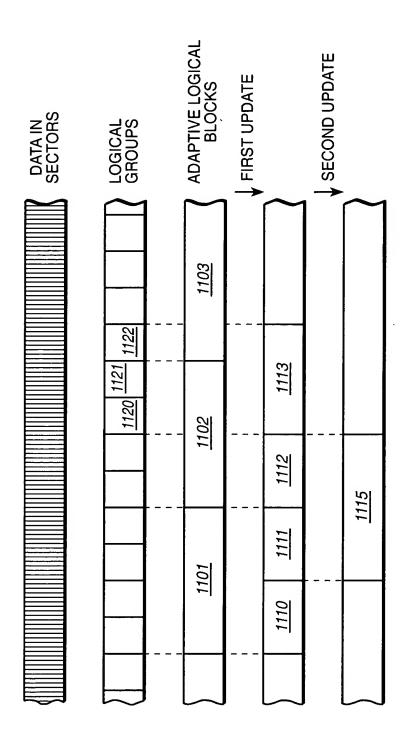


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LOGICAL ADDRESS SPACE

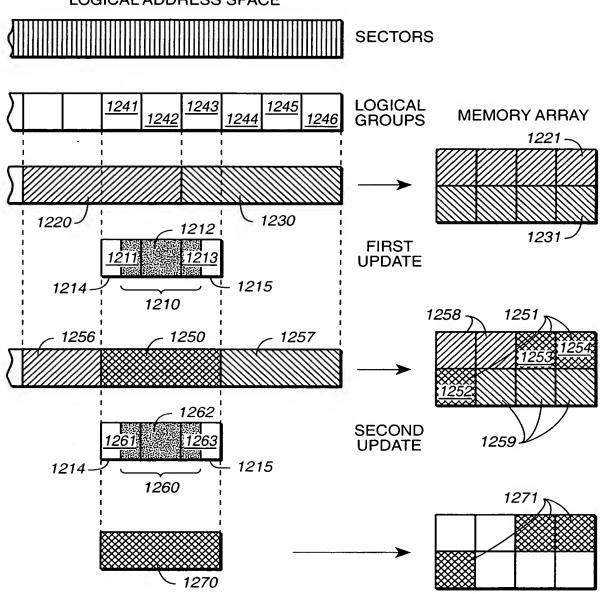
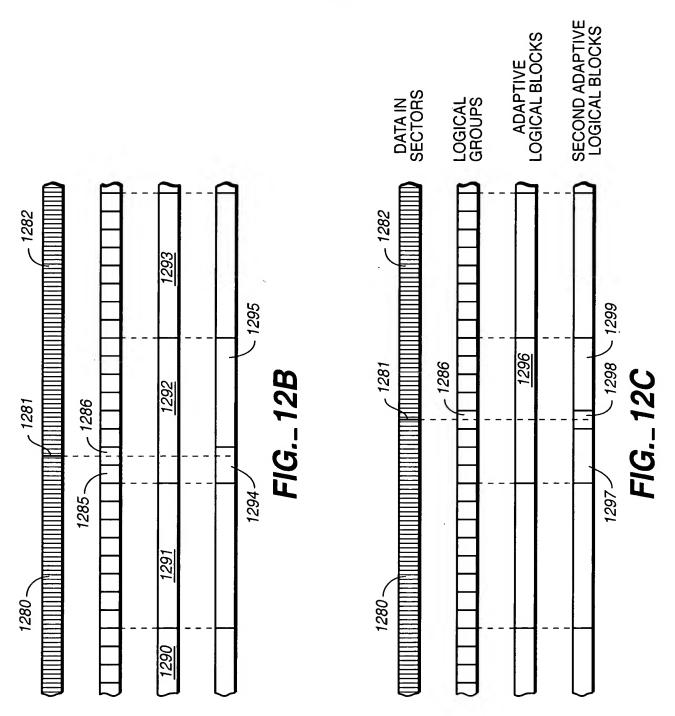


FIG._12A



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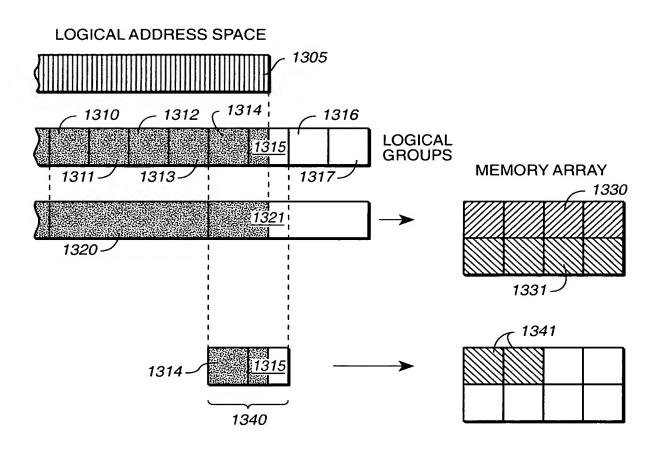


FIG._13

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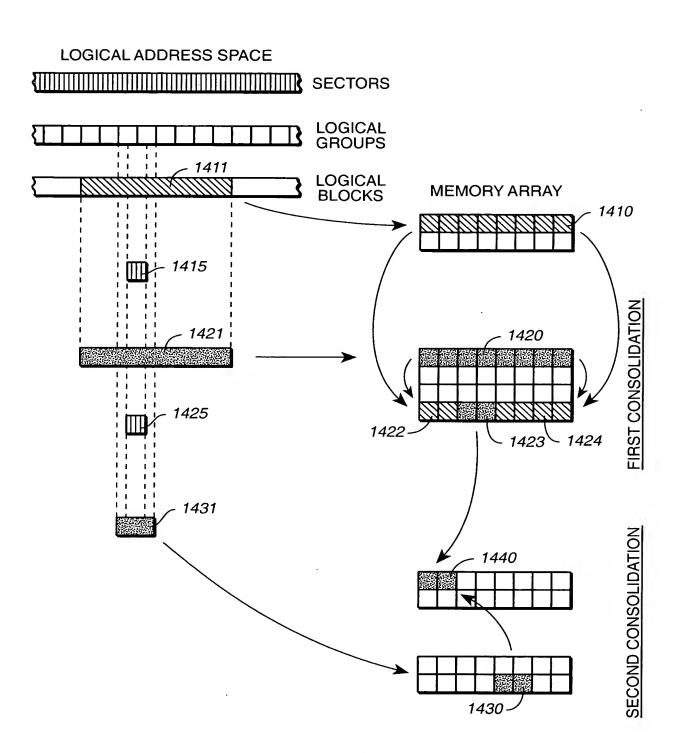


FIG._14

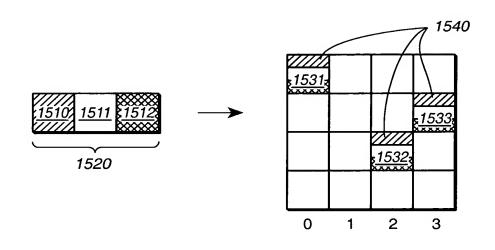


FIG._15A

MEMORY ARRAY

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		8 9 10 11	20 21 22 23	n-4 n-3 n-2 n-1	1533	4 5 6 7	16 17 18 19	•••	n-8 n-7 n-6 n-5	1532	
0 1 2 3 12 13 14 15 : : n-12 n-11 n-10 n-9	1531										

PLANE 3

PLANE 2

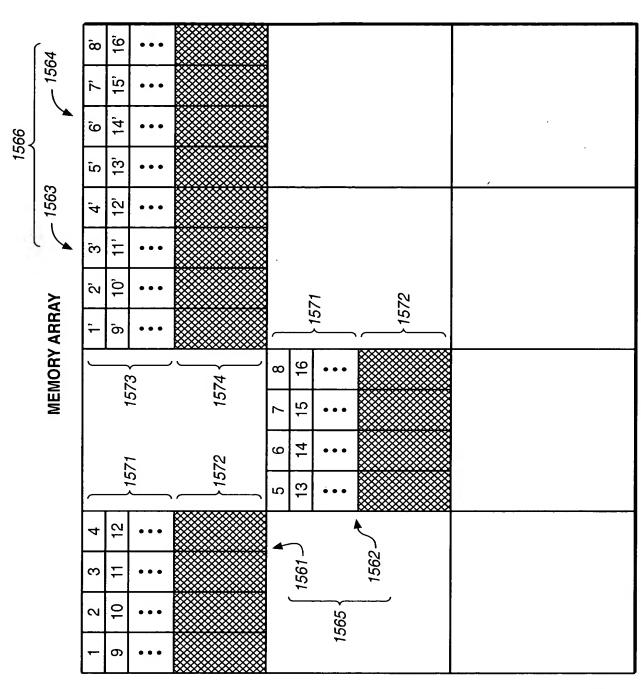
PLANE 1

PLANE 0

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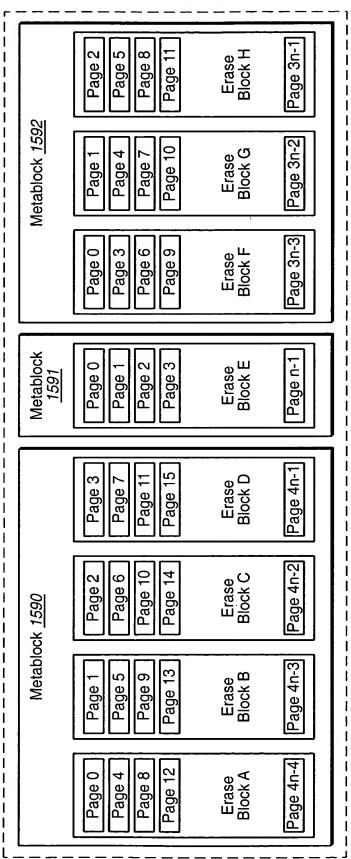
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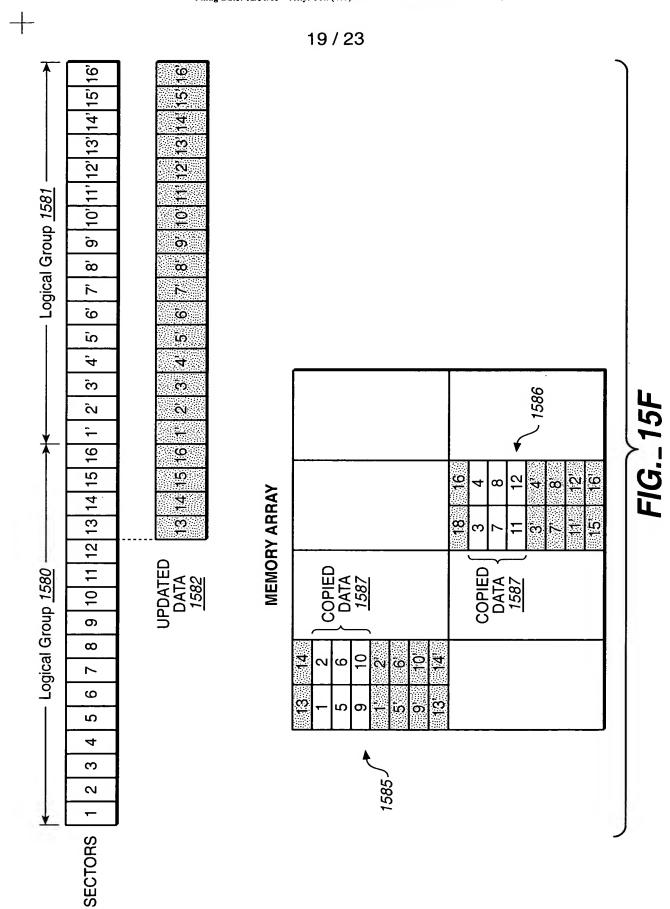
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PROGRAM BLOCK

FIG._ 15E



1_

LOGICAL GROUP	SIZE	LOGICAL GROUP No.	BLOCK
L1	3	1	Α
L2	3	2	В
L3	3	3	С

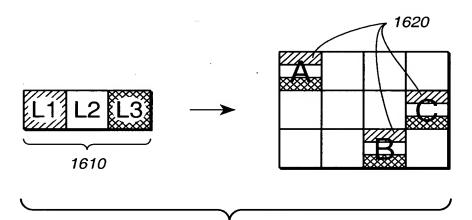
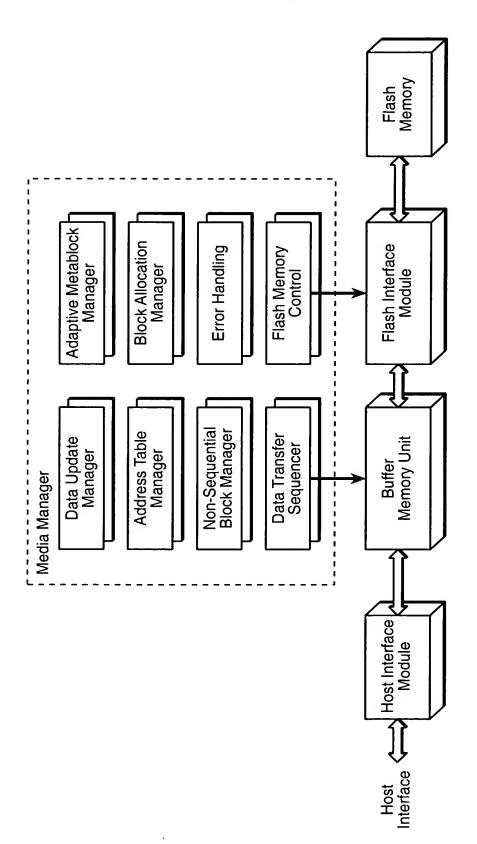


FIG._16

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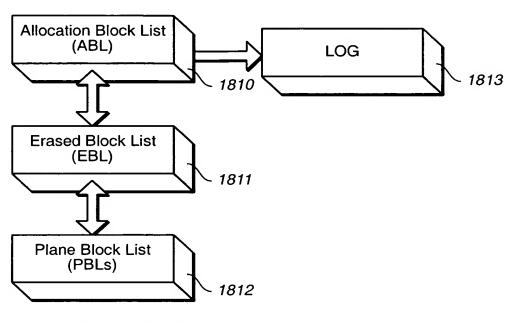


FIG._18A

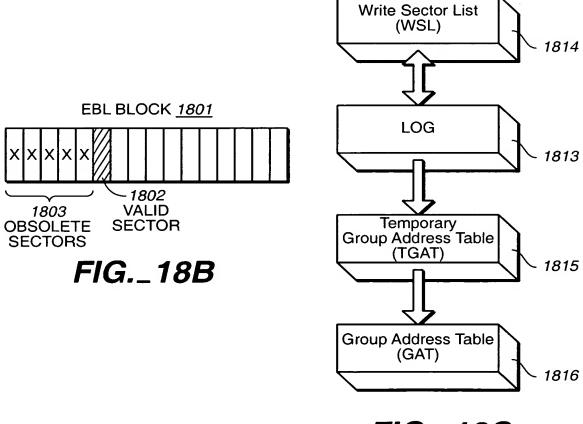


FIG._18C

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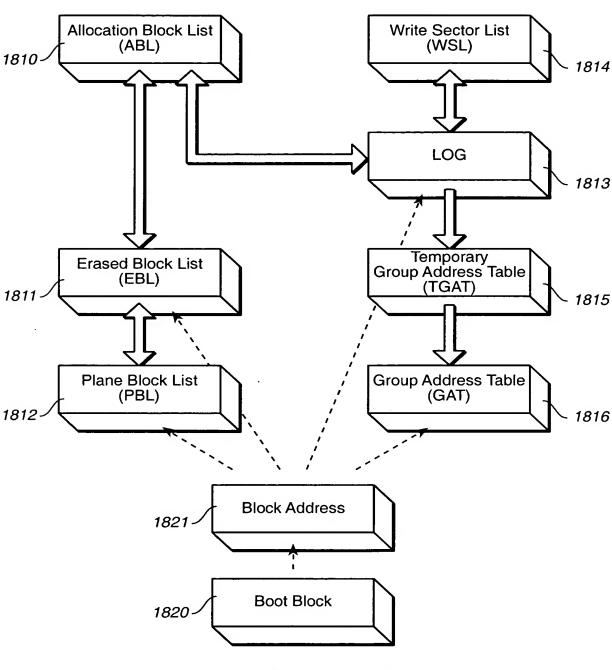


FIG._18D